CLAIMS

1. A method of forming a pitcher-shaped active area structure for a field effect transistor (FET), the method comprising the steps of:

forming divots into top portions of side walls of at least two shallow trench insulator (STI) structures formed into a substrate and that isolate a FET and define an active area structure; and

migrating substrate material into at least portions of the divots, thereby forming a widened top portion of the active area structure with a larger width than a bottom portion of the active area structure.

2. The method of claim 1, wherein the step of forming divots into top portions of side walls of at least two STI structures comprises the step of implementing a wet etch to remove the top portions of the sidewalls of the at least two STI structures, thereby forming divots in the top portions of the sidewalls of the at least two STI structures.

3. The method of claim 1, wherein the step of migrating substrate material into at least portions of the divots comprises the step of implementing a hydrogen annealing technique to migrate substrate material into at least portions of the divots, thereby forming a widened top portion of the active area structure with a larger width than a bottom portion of the active area structure.

4. The method of claim 3, wherein the step of implementing a hydrogen annealing technique to migrate substrate material into at least portions of the divots further comprises the step of rounding top corners of the widened top portion of the active area structure.

5. A method of forming a pitcher-shaped active area structure for a field effect transistor (FET), the method comprising:

implementing a wet etch to remove a pad oxide layer formed on a substrate and portions of an STI oxide fill and STI liner oxide that form top portions of sidewalls of at least two shallow trench insulator (STI) structures that isolate a FET and define an active area structure, thereby forming divots in the top portions of the sidewalls of the at least two STI structures; and

implementing a hydrogen annealing technique to migrate substrate material into at least portions of the divots, thereby forming a widened top portion of the active area structure with a larger width than a bottom portion of the active area structure.

6. The method of claim 5, wherein the step of implementing a wet etch comprises the step of implementing a buffered hydrogen fluoride acid (BHF) etch to remove the pad oxide layer and portions of the STI oxide fill and the STI liner oxide that form the top portions of the sidewalls of the at least two STI structures, thereby forming divots in the top portions of the sidewalls of the at least two STI structures.

7. The method of claim 5, wherein the step of implementing a wet etch comprises the step of implementing an isotropic plasma etch to remove the pad oxide layer and portions of the STI oxide fill and the STI liner oxide that form the top portions of the sidewalls of the at least two STI structures, thereby forming divots in the top portions of the sidewalls of the at least two STI structures.

8. The method of claim 5, wherein the step of implementing a wet etch is performed with a 40/1 etch chemistry and in the range of approximately 1 to 2 minutes.

9. The method of claim 5, wherein the step of implementing a wet etch forms divots with a depth of approximately 500 Å or less.

10. The method of claim 5, wherein the step of implementing a hydrogen annealing technique to migrate substrate material into at least portions of the divots further comprises the step of rounding top corners of the widened top portion of the active area structure.

11. The method of claim 5, wherein the step of implementing a hydrogen anneal is performed at a temperature of 700°C. or higher.

12. The method of claim 5, wherein the step of implementing a hydrogen anneal is performed under a pressure of 10^{-3} Torr or higher.

13. A pitcher-shaped active area structure for a field effect transistor (FET) comprising:
a semiconductor substrate; and
at least two shallow trench insulator (STI) structures formed into the substrate that isolate the FET and define an active area structure, the active area structure comprising:
a widened top portion; and
a bottom portion, wherein the widened top portion has a larger width than the bottom portion.

14. The structure of claim 13 further comprising a pad oxide layer formed on the substrate, and wherein the at least two STI structures are formed into the substrate through the pad oxide layer, the at least two STI structures comprising an STI oxide liner and an STI oxide fill formed on the STI oxide liner.

15. The structure of claim 13, wherein the at least two STI structures comprise divots in top portions of side walls of the at least two STI structures into which the widened top portion of the active area structure extends.

16. The structure of claim 15, wherein the semiconductor substrate comprises silicon, and wherein the widened top portion formed into divots comprises single crystalline silicon.

17. The structure of claim 15, wherein the divots comprise a depth of approximately 500 Å or less.

18. The structure of claim 13, wherein the widened top portion of the active area structure further comprises rounded top corners.

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